What is claimed is:

1. A method of creating a semiconductor device package, comprising the step of:

providing a semiconductor device, said device having been provided with points of electrical contact in an active surface thereof, said points of electrical contact having been provided with fine pitch, high reliability solder bumps, said solder bumps extending from said active surface of said semiconductor device over a height of columns of pillar metal, said columns of pillar metal being in contact with said points of electrical contact provided in the active surface of said semiconductor device;

providing a Ball Grid Array substrate, said BGA substrate having been provided with points of electrical contact over a first and a second surface thereof, said points of electrical contact provided over the second surface of said BGA substrate being connected to interconnect lines provided over the second surface of said BGA substrate;

providing a solder mask over said second surface of said BGA substrate;

positioning said device over the second surface of said BGA substrate, said fine pitch, high reliability solder bumps facing said second surface of said BGA substrate, providing contact between said fine pitch, high reliability solder bumps and said

points of electrical contact provided over said second surface of said BGA substrate;

establishing electrical contact between said fine pitch, high reliability solder bumps and said points of electrical contact provided over said second surface of said BGA substrate by a process of solder reflow;

cleaning flux that has been accumulated in a gap between the active surface of the semiconductor device and the second surface of the BGA substrate;

encapsulating said semiconductor device in a molding compound, said molding compound surrounding said device on all sides including said active surface of said device;

inserting contact balls into said points of electrical contact provided over said first surface of said BGA substrate; and

establishing electrical contact between said solder balls inserted into said solder mask provided over said first surface of said BGA substrate and said points of electrical contact provided over said first surface of said BGA substrate by a process of solder reflow.

2. The method of claim 1 wherein said solder mask provided over said second surface of said BGA substrate is removed from said points of electrical contact provided over the second surface of

said BGA substrate by a measurable amount, creating a channel through which cleaning solution can readily flow.

3. The method of claim 1 wherein said points of electrical contact provided in an active surface of said device comprise a peripheral pad design.

4. The method of claim 1 wherein said points of electrical contact provided in an active surface of said device comprise a center type pad design.

5. The method of claim 4 wherein dummy solder bumps are provided over the active surface of said device, providing mechanical support for said device, said dummy solder bumps being provided in addition to said fine pitch, high reliability solder bumps provided to said points of electrical contact in the active surface of said device.

6. The method of claim 1 wherein said providing fine pitch, high reliability solder bumps to said device comprising the steps of:

depositing a layer of dielectric over the active surface of said device;

patterning and etching said layer of dielectric, creating openings in said layer of dielectric in a pattern overlying said

points of electrical contact in an active surface of said device, exposing the surface of said points of electrical contact in an active surface of said device;

depositing a layer of passivation over the surface of said layer of dielectric, including the exposed surface of said points of electrical contact in an active surface of said device;

patterning and etching said layer of passivation, creating openings in said layer of passivation in a pattern overlying said points of electrical contact in an active surface of said device, exposing the surface of said points of electrical contact in an active surface of said device;

depositing a layer of metal barrier over the surface of said layer of passivation, including the exposed surface of said points of electrical contact in an active surface of said device;

creating pillar metal and solder bumps overlying said layer of barrier metal in a pattern that pattern overlying said points of electrical contact in an active surface of said device, said pillar metal and solder bumps being separated by a layer of under bump metal; and

etching said layer of barrier metal.

7. The method of claim 6 wherein said etching said layer of barrier metal is applying an isotropic etching process, removing

said barrier metal from the surface of said layer of passivation where said barrier layer is not covered by said pillar metal.

8. The method of claim 6 wherein said etching said layer of barrier metal is applying an anisotropic etching process, removing said barrier metal from the surface of said layer of passivation where said barrier layer is not shielded from said anisotropic etch by said solder bump.

9. The method of claim 1, said points of electrical contact provided in an active surface of said device having a pitch of about 200 μm or less.

10. The method of claim 1 with an additional step of flux removal from a gap between said second surface of said BGA substrate and said active surface of said semiconductor device, said additional step being performed after completion of flip chip assembly and solder reflow.

11. The method of claim 1, said step of encapsulating said semiconductor device in a molding compound being replaced with a step of providing underfill for said device, said step being performed after said step of establishing electrical contact between said fine pitch, high reliability solder bumps and said

points of electrical contact provided over said second surface of said BGA substrate by a process of solder reflow.

12. The method of claim 1, said height of columns of pillar metal being between about 10 and 100 μm and more preferably about 50 μm.

13. A semiconductor device package, comprising:

a semiconductor device, said device having been provided with points of electrical contact in an active surface thereof, said points of electrical contact having been provided with fine pitch, high reliability solder bumps, said solder bumps extending from said active surface of said semiconductor device over a height of columns of pillar metal, said columns of pillar metal being in contact with said points of electrical contact provided in the active surface of said semiconductor device;

a Ball Grid Array substrate, said BGA substrate having been provided with points of electrical contact over a first and a second surface thereof, said points of electrical contact provided over the second surface of said BGA substrate being connected to interconnect lines provided over the second surface of said BGA substrate;

a solder mask provided over said second surface of said BGA substrate;

said device being positioned over the second surface of said BGA substrate, said fine pitch, high reliability solder bumps facing said second surface of said BGA substrate, providing contact between said fine pitch, high reliability solder bumps and said points of electrical contact provided over said second surface of said BGA substrate;

electrical contact having been established between said fine pitch, high reliability solder bumps and said points of electrical contact provided over said second surface of said BGA substrate by a process of solder reflow;

said semiconductor device being encapsulated in a molding compound, said molding compound surrounding said device on all sides including said active surface of said device;

contact balls making electrical contact with said points of electrical contact provided over said first surface of said BGA substrate; and

electrical contact having been established between said solder balls inserted into said solder mask provided over said first surface of said BGA substrate and said points of electrical contact provided over said first surface of said BGA substrate by a process of solder reflow.

14. The semiconductor device package of claim 13, said solder mask provided over said second surface of said BGA substrate

being removed from said points of electrical contact provided over the second surface of said BGA substrate by a measurable amount, creating a channel through which cleaning solution can readily flow.

15. The semiconductor device package of claim 13, said points of electrical contact provided in an active surface of said device comprising a peripheral pad design.

16. The semiconductor device package of claim 13, said points of electrical contact provided in an active surface of said device comprising a center type pad design.

17. The semiconductor device package of claim 16, dummy solder bumps having been provided over the active surface of said device, providing mechanical support for said device, said dummy solder bumps being provided in addition to said fine pitch, high reliability solder bumps provided to said points of electrical contact in the active surface of said device.

18. The semiconductor device package of claim 13, said fine pitch, high reliability solder bumps provided to said device comprising:

a layer of dielectric deposited over the active surface of said device, openings having been created in said layer of dielectric in a pattern overlying said points of electrical contact in an active surface of said device, exposing the surface of said points of electrical contact in an active surface of said device;

a layer of passivation deposited over the surface of said layer of dielectric, including the exposed surface of said points of electrical contact in an active surface of said device, openings having been created in said layer of passivation in a pattern overlying said points of electrical contact in an active surface of said device, exposing the surface of said points of electrical contact in an active surface of said device;

a layer of metal barrier deposited over the surface of said layer of passivation, including the exposed surface of said points of electrical contact in an active surface of said device;

pillar metal and solder bumps overlying said layer of barrier metal in a pattern overlying said points of electrical contact in an active surface of said device, said pillar metal and solder bumps being separated by a layer of under bump metal; and

said layer of barrier metal having been etched.

19. The semiconductor device package of claim 18, said etching said layer of barrier metal having removed said barrier metal from the surface of said layer of passivation where said barrier layer is not covered by said pillar metal.

20. The semiconductor device package of claim 18, said etching said layer of barrier metal having removed said barrier metal from the surface of said layer of passivation where said barrier layer is not covered by said pillar metal while further leaving in place said barrier layer extending from said pillar metal by a measurable amount.

21. The semiconductor device package of claim 13, said points of electrical contact in an active surface of said device having a pitch of about 200 μm or less.

22. The semiconductor device package of claim 13, flux removal from a gap between said second surface of said BGA substrate and said active surface of said semiconductor device having been performed after completion of flip chip assembly and solder reflow.

23. The semiconductor device package of claim 13, said encapsulation of said semiconductor device in a molding compound being replaced with an underfill for said device.

24. The semiconductor device package of claim 13, said height of columns of pillar metal being between about 10 and 100 μm and more preferably about 50 μm.